



Eur päisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 0 795 812 A1

(12)

EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:

17.09.1997 Bulletin 1997/38

(51) Int. Cl.⁶: G06F 3/06

(21) Application number: 95936768.1

(86) International application number:
PCT/JP95/02299

(22) Date of filing: 10.11.1995

(87) International publication number:
WO 96/15488 (23.05.1996 Gazette 1996/23)

(84) Designated Contracting States:
DE FR GB

(30) Priority: 11.11.1994 JP 277422/94

(71) Applicant: HITACHI, LTD.
Chiyoda-ku, Tokyo 101 (JP)

(72) Inventors:

- ICHIKAWA, Masatoshi
Hachimanyama-Apato 552
Yokohama-shi Kanagawa 244 (JP)
- ISONO, Soichi
Sagamihara-shi Kanagawa 228 (JP)

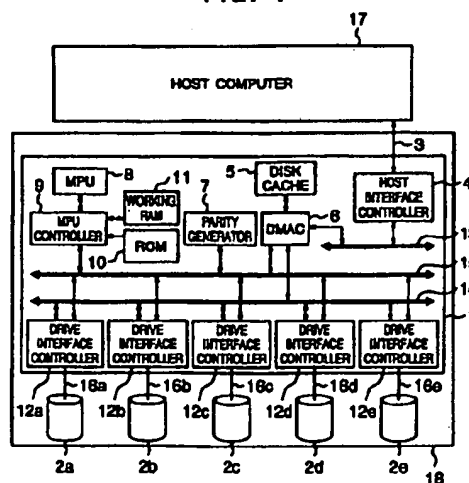
- HONDA, Kiyoshi
Beruhaimu I - 105
Yokohama-shi Kanagawa 244 (JP)
- MATSUMOTO, Jun
Tokyo 158 (JP)
- IWASAKI, Hidehiko
Hiratsuka-shi Kanagawa 259-12 (JP)

(74) Representative: Altenburg, Udo, Dipl.-Phys. et al
Patent- und Rechtsanwälte,
Bardehle, Pagenberg, Dost, Altenburg,
Frohwitter, Geissler & Partner,
Gallieplatz 1
81679 München (DE)

(54) DISK ARRAY CONTROLLER AND DISK ARRAY DEVICE

(57) A disk array controller or a disk array system includes a disk array control unit having an MPU 8 and a user data transfer control unit having host interfaces 3 and 4 with a host computer 17, a memory 5 for temporarily storing data, a redundant data generator 7 for generating redundant data, multi-channel disk device interfaces 16a~16e and 12a~12e and a data transfer control circuit (DMAC) 6 for controlling the data transfer between the host interface, the memory, the redundant data generator and the disk device interface. Internal buses are of at least three-bus structure including a control bus (for MPU) 15, a host data bus 13 and a drive data bus 14.

FIG. 1



EP 0 795 812 A1